REMARKS

Applicant was required to divide FIGS. 5 and 7 into two sheets and FIG. 9 into three sheets. The specification has been amended to reflect such change.

The paragraph on page 6, beginning on line 3 and continuing to line 6, is being deleted by this amendment, since it was inserted inadvertently. The substance of the paragraph appears correctly on page 12, beginning on line 16 and continuing to line 19.

The Assistant Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 500845.

Respectfully submitted,

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Date

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Attachment: 7 sheets of Specification changes with markings showing changes made.

VERSION OF SPECIFICATION PARAGRAPHS WITH MARKINGS SHOWING CHANGES MADE

Delete the Paragraph on Page 6, beginning at line 3.

~~Also one the director board 20_4 is a common memory 64, here a non-volatile SRAM shown in more detail in FIG. 8. Thus, it is noted that the four CPUs, 48_1-48_4 described above in connection with FIG. 7 are shown also coupled to the common memory 64. Here, the four CPUs, 48_1-48_4 are also designated as CPU A - CPU D, respectively.~~

Change to the Paragraphs beginning on Page 9 at line 11.

FIGS. 5A and 5B ~~is~~ are a four bus data storage system having ESCON front end adapters and front end directors according to the invention;

FIG. 6 is an isometric sketch of an interface used in the system of FIGS. 5A and 5B;

FIGS. 7A and 7B ~~is~~are a block diagram of one of the ESCON front end adapters and one of the front end directors used in the system of FIG. 5 in accordance with the invention;

FIG 8 is a block diagram of a system for enabling processors of the system of FIGS. 7A and 7B having the same software program to transparently access a common memory;

FIGS. 9A, 9B and 9C ~~is~~are a more detailed block diagram of FIG. 8;

FIG. 10 is a diagram showing the addresses which are provided by a processor used in the system of FIGS. 9A, 9B and 9C;

Change to the Paragraph beginning on Page 10 at line 9.

Referring now to FIGS. 5A and 5B, a data storage system 10 is shown wherein a host computer 12 is coupled to a bank 14 of disk drives through a system interface 16. The system interface 16 includes a cache memory 18, having high address memory sections 18H and low address memory sections 18L. A plurality of directors 20_0-20_{15} is provided for controlling data transfer between the host computer 12 and the bank 14 of disk drives as such data passes through the cache memory 18. A pair of high address busses TH, BH is electrically connected to the high

address memory sections 18H. A pair of low address busses TL, BL electrically connected to the low address memory sections 18L. The cache memory 18 has a plurality of storage location addresses. Here, the storage locations having the higher addresses are in the high address memory sections 18H and the storage locations having the lower addresses are in the low address memory sections 18L. It should be noted that each one of the directors 20_0-20_{15} is electrically connected to one of the pair of high address busses TH, BH and one of the pair of low address busses TL, BL. Thus, each one of the directors 20_0-20_{15} is able to address all locations in the entire cache memory 18 (i.e., to both the high address memory sections 18H and the low address memory sections 18L) and is therefore able to store data in and retrieve data from any storage location in the entire cache memory 18.

Change to the Paragraph beginning on Page 11 at line 26.

Referring now to FIGS. 7A and 7B, an exemplary one of the front end I/O adapter printed circuit boards, here I/O adapter board 22_4 and its associated (i.e., coupled) front end director board, here director board 24_4 are shown in more detail. It is first noted that here the front end I/O adapted board 22_4 is an ESCON front end adapter board having four ports H1, H2, H3 and H4 adapted for coupling to the host computer. The front end I/O adapter board 20_4 has four optic interfaces 40_1-40_4, each one being connected to a corresponding one of the four ports H1, H2, H3 and H4. The adapter board 22_4 also includes four gate arrays 42_1-42_4, each one coupled to a corresponding one of the optic interfaces 40_1-40_4, respectively. The front end adapted printed circuit board 22_4 also includes four separate CPUs 44_4, each one controlling a corresponding one of the gate arrays 42_1-42_4, respectively and the one of the optic interfaces 40_1-40_4, respectively, coupled to such corresponding one of the gate arrays 42_1-42_4, as indicated. Thus, four independent (i.e., concurrent) data channels DMA channels, i.e., Channel A, Channel B, Channel C and Channel D, are provided.

Change to the Paragraph beginning on Page 13 at line 4.

Also included on the director board is a common, shared memory 64, here a non-volatile SRAM. The memory 64 is coupled to the four CPUs 48_1-48_4, as shown more clearly in FIG. 8. In FIG. 8, the four CPUs 48_1-48_4 are also designated as CPU A -CPU D, respectively. It is first noted that the four CPUs A-D are coupled to other director boards in the system via a system Ethernet hub, not shown. Each one of the four CPUs A-D are coupled to DATA and address busses via a corresponding one of four personal address translators 70_1-70_4, respectively, as shown. The data and addresses on the data and addresses busses are fed to the memory 64 via a common translator arbiter72, as indicated. The details of the arrangement shown in FIG, 8 will be described in connection with FIGS. 9A, 9B and 9C. Suffice it to say here, however, that various messages, such as error messages and interrupts from the other directors may come into an Ethernet controller 68 or may be communicated from this director board to the other directors via the Ethernet controller 68. In any event, considering for example the case where a message is received by the Ethernet controller 68. This message is routed to a master one of the CPUs A-D, here to CPU A. The message is then transferred to a DRAM 74 coupled to the CPU A. It is noted that each one of the CPUs A-d has its own cache memory. Each cache memory stores the same program. One function of the program is to enable the CPU to write data into, or read data from a specific region in the memory 64 designated for that CPU. Thus, referring to FIGS. 9A, 9B and 9C, it is noted that each one of the CPUs has a corresponding region in the memory. Further, it is noted that here the address to the memory is a 23 bit word. Each one of the CPU regions is designated by the 7 most significant bits (MSBs) of the address presented to the memory 64. Thus, here for example, addresses (i.e., memory locations) having as the 7 MSBs addressees 0-77,fff (hex) are designated as the CPU A memory region; addresses 78,000-ef,fff (hex) are designated as the CPU B memory region, addresses f0,000-167,000 (hex) are designated as the CPU C memory region, and addresses 168,000-1df,fff (hex) are designated as the CPU D memory region. A shared memory region having as the 7 MSBs addresses 1e0,000-1ff,fff (hex) is also provided for reasons to be described.

Change to the Paragraph beginning on Page 18 at line 7.

It is next noted that as shown in FIGS. 9A, 9B and 9C, it is desired that the CPU memory regions and the shared memory region be contiguous. That is, it is desired that the memory region from 0-1f,fff be used for storage of data from the four CPUs A-D. However, referring also to FIG. 10, it is noted that here only a portion of the available addresses for each CPU are actually used. For example, while address from 00,000-df,fff are available for "OWN CPU", here only addresses 00,000-77,fff (hex) are actually used. Addresses 78,000-df,fff (hex) are reserved for further expansion. Thus, the currently used addresses are designated as (p) in FIG. 10 and the reserved, unused , addresses are designated as (ΔG). The addresses used by the shared memory region are designates by S. It should be noted therefore, that there is a gap, G, between the last used address for one CPU and the first address used by the next CPU.

Changes to the Paragraphs beginning on Page 21 at line 20.

Referring now again to FIGS. 9A, 9B and 9C, it is noted that each one of the CPUs A-D may issue an attention other (ATT_OTH) command to any other one of the CPUs A-D in a uni-cast mode of operation, or may issue such command to all the other CPUs A-D in a broadcast mode of operation. Further, the common address translator/arbiter may issue an interrupt command (INT) at the request of one of the CPUs A-D to any other one of the CPUs A-D in a uni-cast mode of operation, or may issue such command to all CPUs A-D in a broadcast mode of operation. Still further, the common address translator/arbiter may issue a reset command (RST) at the request of one of the CPUs A-D to any other one of the CPUs A-D in a uni-cast mode of operation, or may issue such command to all the other CPUs A-D in a broadcast mode of operation.

More particularly, and referring again to FIGS. 9A, 9B and 9C, each one of the personal address translators 70_1-70_4 is fed with a two bit binary code, here a two bit voltage level on each of a two line bus IDA, IDB, IDC and IDD, respectively, as shown, to thereby provide each one of the translators 70_1-70_4, respectively, with a unique, personal translator ID code. Thus, here the two bit code on buses IDA, IDB, IDC and IDD are: 00, 01, 10, and 11, respectively. Further,

each one of the personal address translators 70_1-70_4 has three ATT_OTH output lines for transmitting an attention other signal to one, or all, of the other personal address translators 70_1-70_4 and one ATT_OTH input line for receiving an attention other signal from one of the other personal address translators 70_1-70_4. Thus, there are four attention other lines. i.e., ATT_OTH_A, ATT_OTH_B, ATT_OTH_C, and ATT_OTH_D. The line ATT_OTH_A is the attention other input line to personal address translator 70_1. The line ATT_OTH_A is connected to the attention other outputs lines ATT_OTH_A of personal address translators 70_2-70_4 in an open-collector configuration. More particularly, the line ATT_OTH_A is coupled to a +V voltage source through a pull-up resistor, R. Thus, in an idle state, the personal address translators 70_2-70_3 produce a "high" (+) voltage on the line ATT_OTH_A thereby producing a "high" voltage on the line ATT_OTH_A. However, if any one of the personal translators 70_2-70_4 (at the request of the CPU B-D, respectively, coupled thereto) issues an attention other command for CPU A, whether in a uni-cast mode just to CPU A or to all other CPUs in a broadcast mode, such CPU issuing the attention other command drives its output ATT_OTH_A line towards ground (i.e., "low), thereby placing a "low" signal on the ATT_OTH_A line to indicate to the personal translator 70_1 that there is an attention command for the CPU A .

Change to the Paragraph beginning on Page 23 at line 21.

For example, if the CPU B issues an attention other command for CPU A, the CPU B issues the attention other command and the ID code for CPU A, here the code 00. The personal translator 70_2 had. in the prior idle state (FIG. 16) generated "high" voltages on its attention other output lines, i.e., ATT_OTH_A, ATT_OTH_C and ATT_OTH_D, FIGS. 9A, 9B and 9C). Once it receives the command from CPU B, the personal translator 70_2 determines whether the command is an attention other command. If it isn't, it returns to the idle state. On the other hand, if it determines that the command is an attention other command, the personal translator 70_2 test whether the command was associated with the same ID code as the CPU B, here 01, or with some other ID code. i.e., 00, 10 or 11. If the ID code associated with the command is the same as the ID code of the personal translator's CPU, here the same as CPU B, 01, all the attention other

lines ATT_OTH_A, ATT_OTH_C and ATT_OTH_D) of the translator 70_2 are driven "low" to thereby transmit an attention other command to all the other CPUs (i.e., CPU A, CPU C and CPU D) in a broadcast mode. If, on the other hand, the ID code with the command is not the same as the ID code of CPU b, in this case. i.e., an ID code 00, or an ID code 10 or an ID code 11), the personal translator 70_2 drives only one of the attention other output lines (either line ATT_OTH_A, or line ATT_OTH_C or line ATT_OTH_D) "low". The particular one of the attention other output lines driven "low" being a function of the ID code in the command. Thus, if the ID code with the command is 00, line ATT_OTH_A is driven "low". If the ID code with the command is 10, line ATT_OTH_C is driven "low". If the ID code with the command is 11, line ATT_OTH_D is driven "low".

Change to the Paragraph beginning on Page 254 at line 16.

Referring now to FIG. 18, a program is stored in the common translator/arbiter 72 (FIGS. 9A, 9B and 9C) for generating the reset command. In response to a rest command issued by one of the CPUs A-D via the data bus thereof and the assert signal from the requesting one of the CPUs, (i.e., a CPU A assert, a CPU B assert, a CPU C assert or a CPU D assert, respectively), the common translator/arbiter 62 will issue a reset command to a designated one of the CPUs to receive such reset command (i.e., either CPU A via a signal on RST_A, or CPU B via a signal on RST_B, or CPU C via a signal on RST_C, or CPU D via a signal on RST_D) in a uni-cast.

Change to the Paragraph beginning on Page 25 at line 6.

Thus, consider for example, the ID code received with the command is ID code 00. Assume also that the CPU A issued the command (i.e., the personal translator 70_1(FIGS. 9A, 9B and 9C) produced a request signal on the CPU A assert line). In such case, a broadcast mode is detected by the common translator 72 and "low" voltages are produced on RESET lines RST_B, RST_C and RST_D. However, in this example, if the ID code received with the command from CPU A had been 10 instead of 00, a uni-cast mode is detected by the common translator 72 and "low" voltage is produced only on RESET line RST_C.

Change to the Paragraph beginning on Page 25 at line 21.

Thus, consider for example, the ID code received with the command is ID code 00. Assume also that the CPU A issued the command (i.e., the personal translator 70_1(FIGS. 9A, 9B and 9C) produced a request signal on the CPU A assert line). In such case, a broadcast mode is detected by the common translator 72 and "low" voltages are produced on RESET lines RST_A, RST_B, RST_C and RST_D. However, in this example, if the ID code received with the command from CPU A had been 10 instead of 00, a uni-cast mode is detected by the common translator 72 and "low" voltage is produced only on RESET line RST_C.